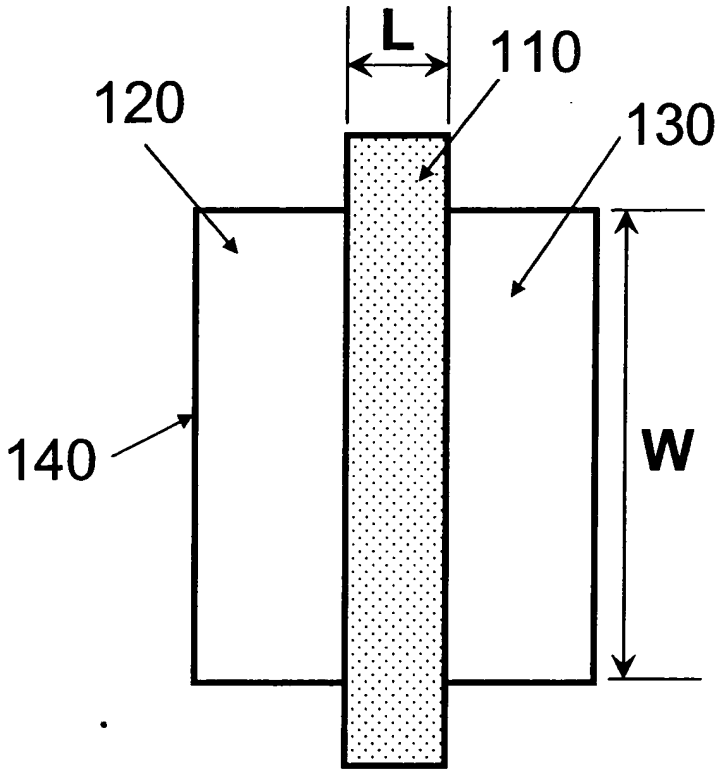
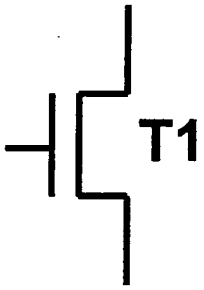
Figure 1
(Prior Art)



Layout

Schematic



T1 model=NMOS L=L0, W=W0

Figure 2
(Prior Art)

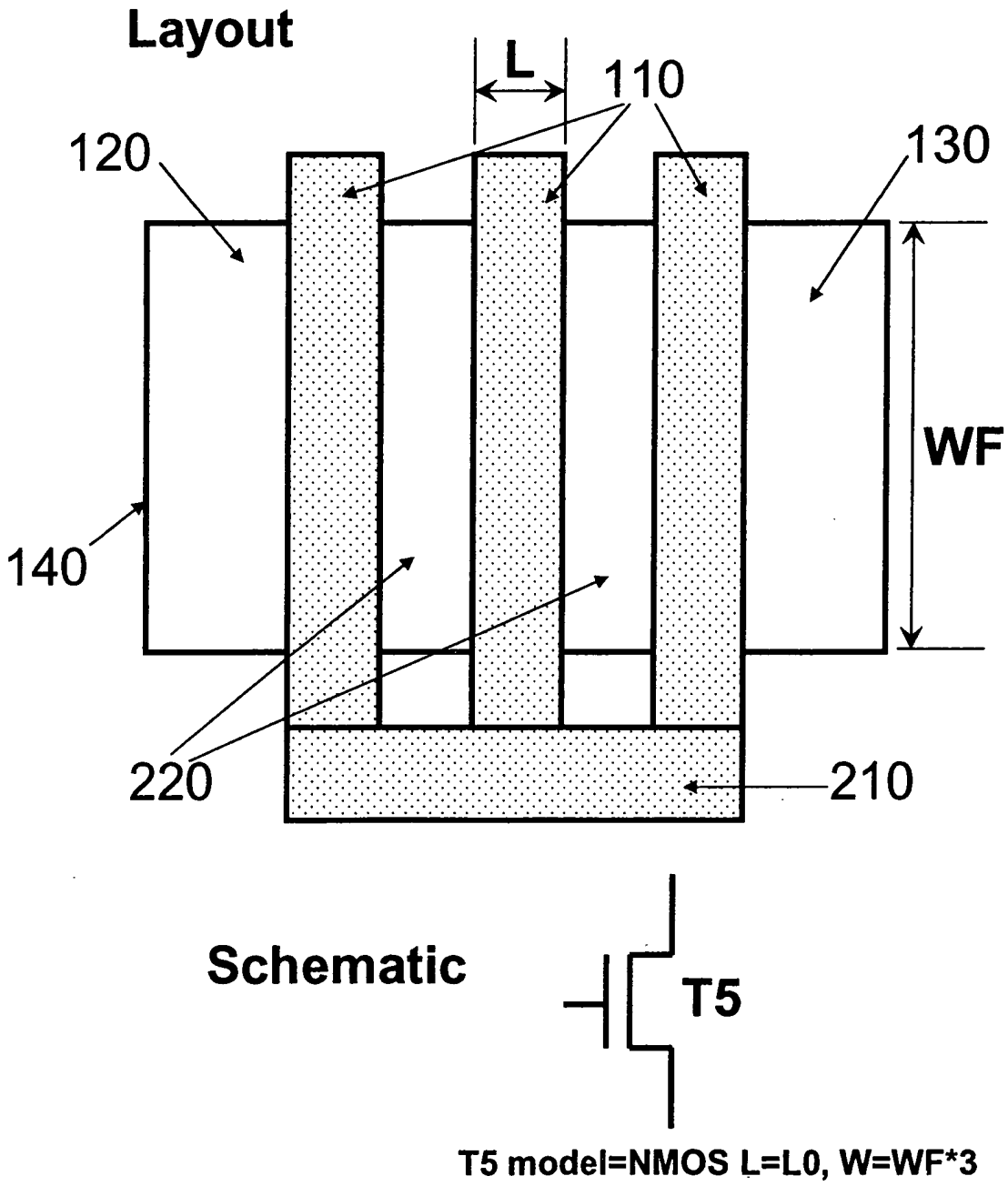


Figure 3
(Prior Art)

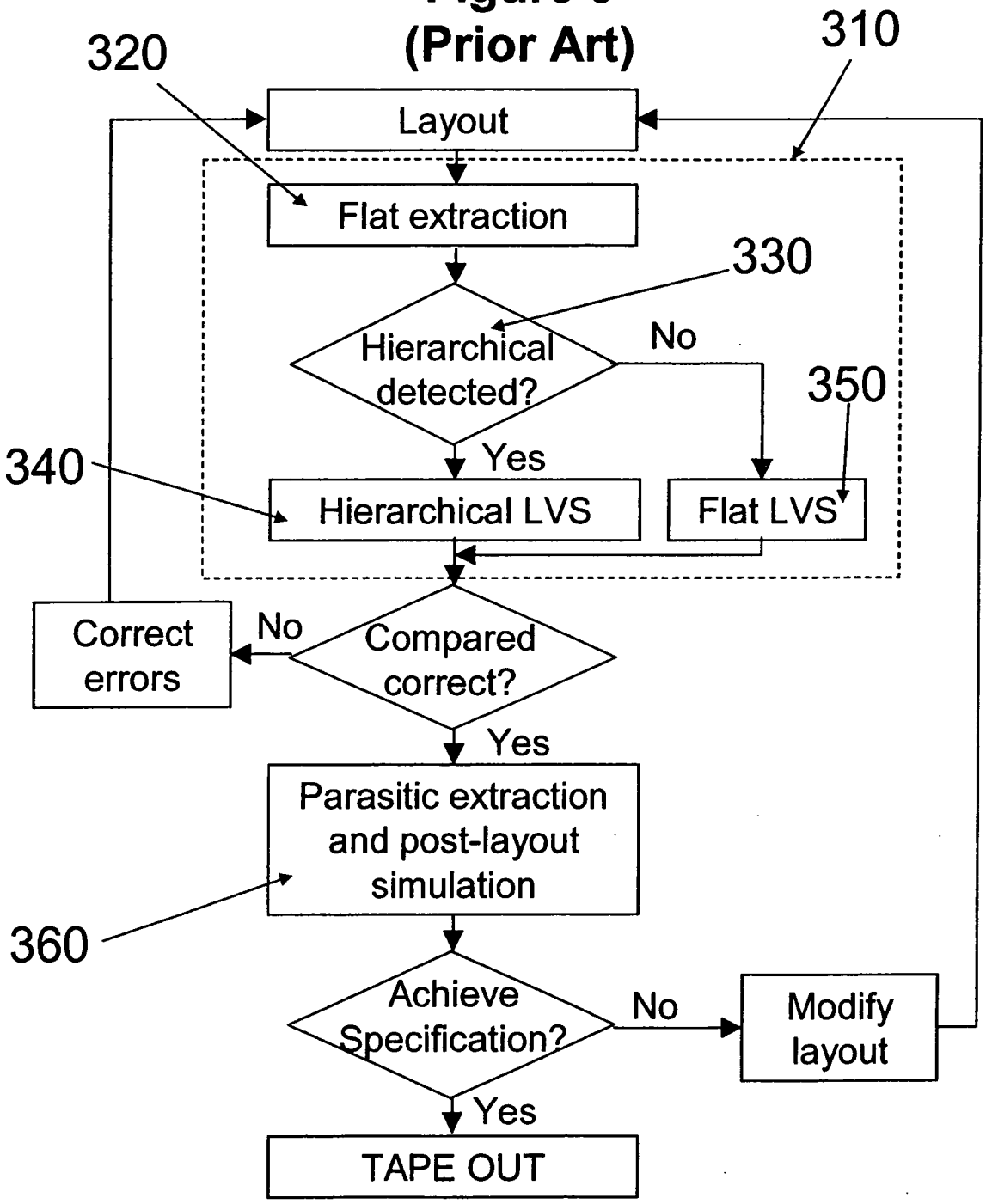


Figure 4

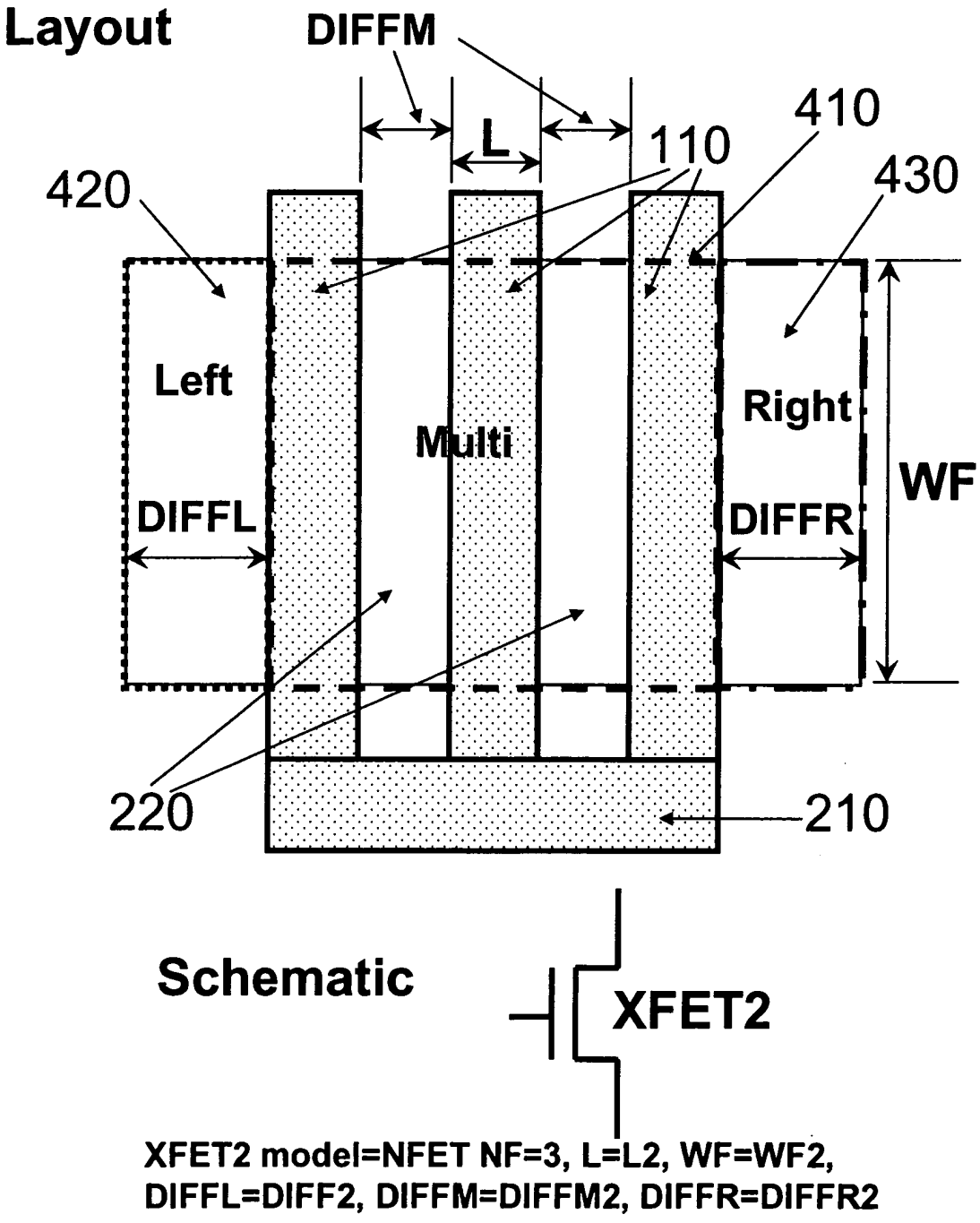

Layout
DIFFM
L
110
410
420
430
Left
Multi
Right
DIFFL
DIFFR
WF
220
210
Schematic
XFET2
XFET2 model=NFET NF=3, L=L2, WF=WF2,
DIFFL=DIFF2, DIFFM=DIFFM2, DIFFR=DIFFR2

Figure 5

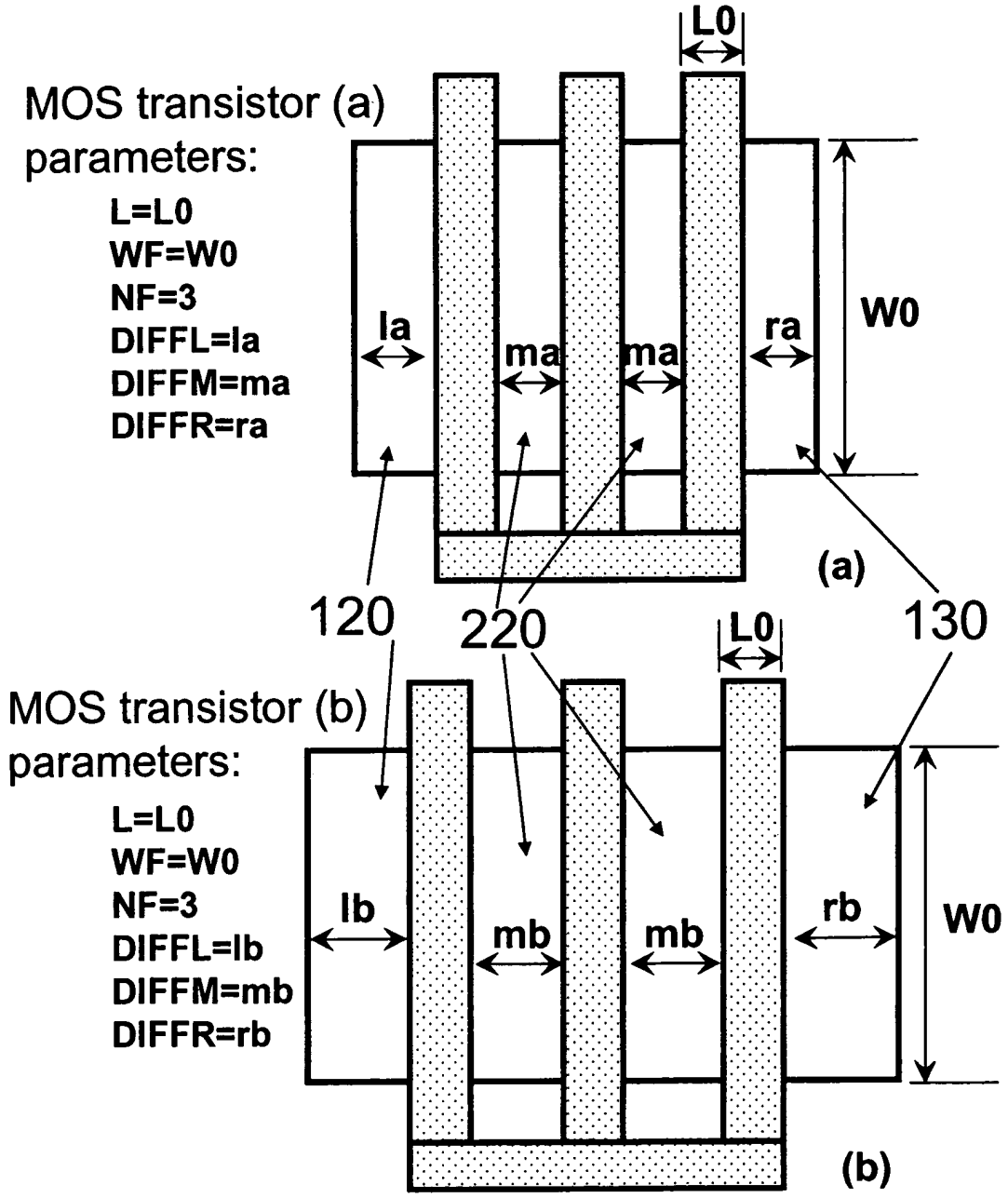

MOS transistor (a) parameters:
L=L0
WF=W0
NF=3
DIFFL=la
DIFFM=ma
DIFFR=ra
L0
la
ma
ma
ra
W0
(a)
120
220
130
MOS transistor (b) parameters:
L=L0
WF=W0
NF=3
DIFFL=lb
DIFFM=mb
DIFFR=rb
L0
lb
mb
mb
rb
W0
(b)

Figure 6

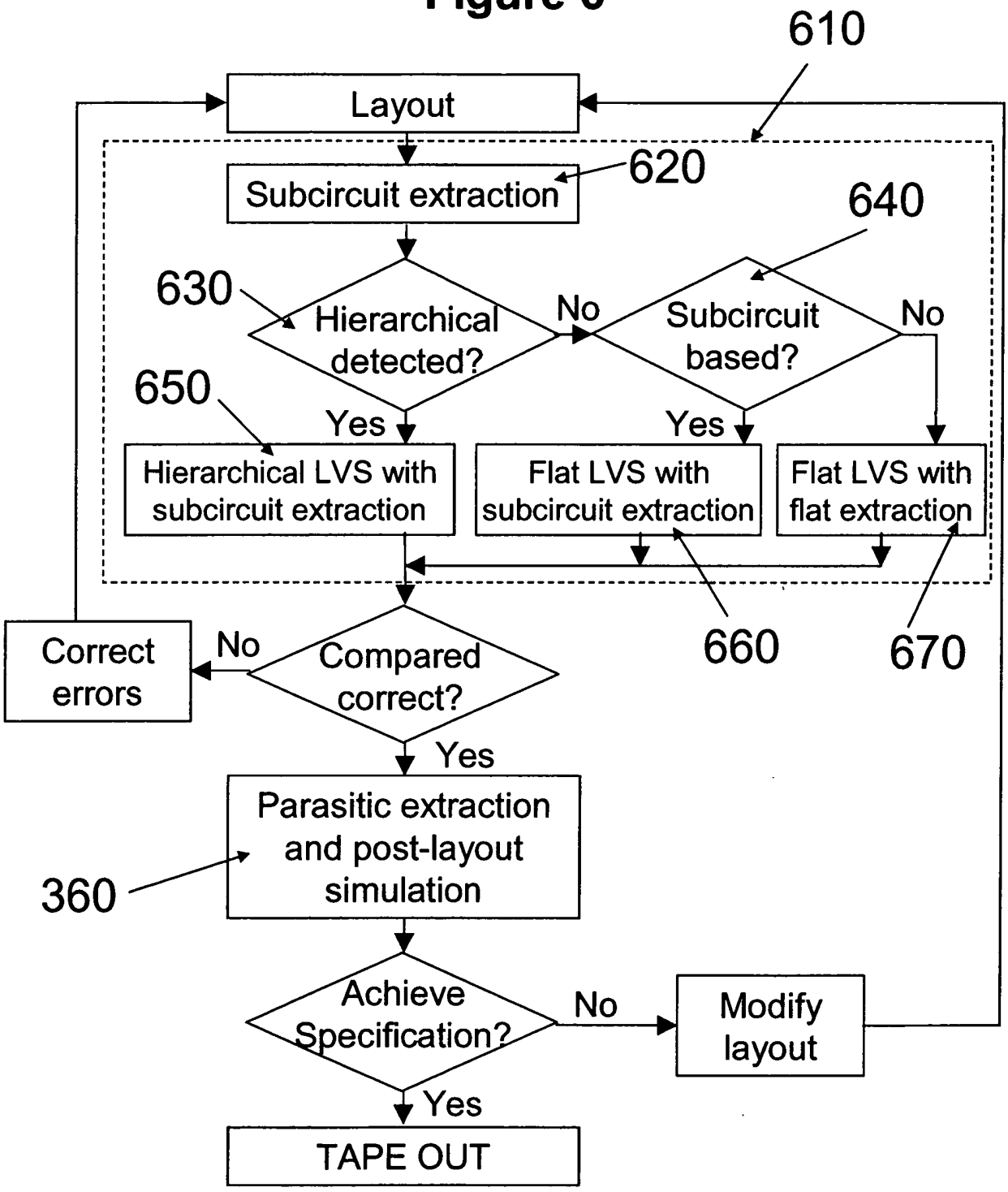
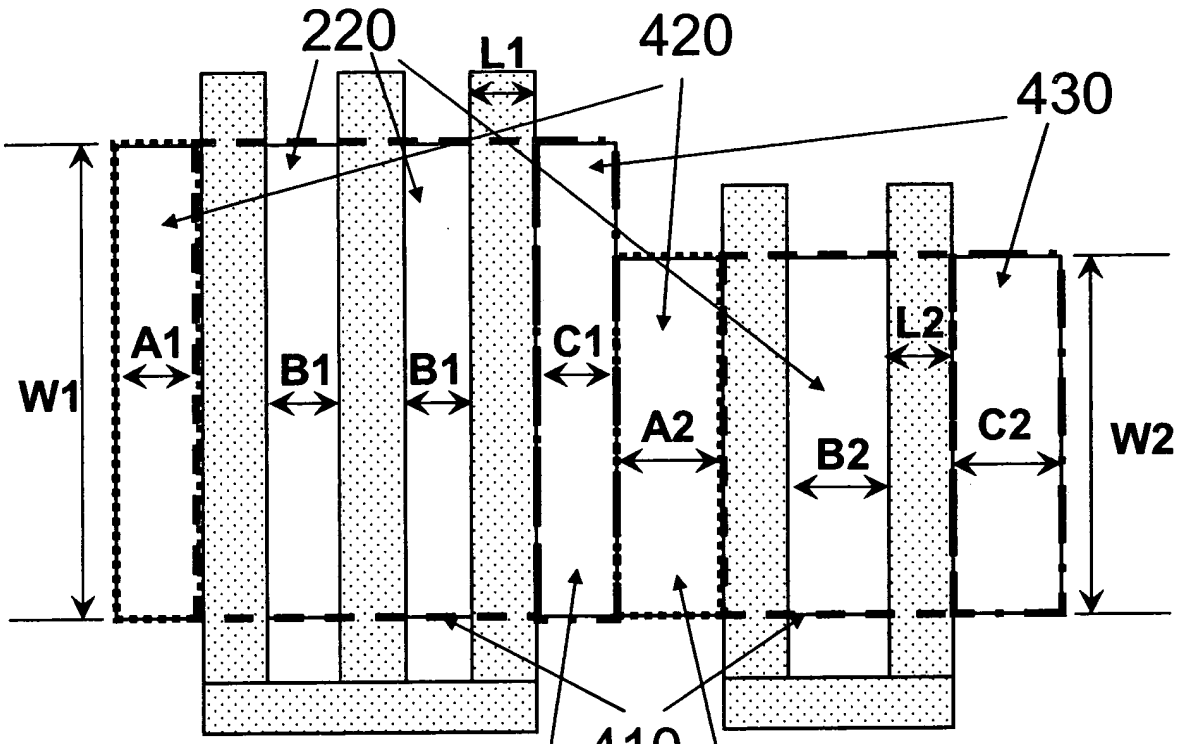

610
Layout
620
Subcircuit extraction
640
630
Hierarchical detected?
No
Subcircuit based?
No
650
Yes
Yes
Hierarchical LVS with subcircuit extraction
Flat LVS with subcircuit extraction
Flat LVS with flat extraction
660
670
Correct errors
No
Compared correct?
Yes
Parasitic extraction and post-layout simulation
360
Achieve Specification?
No
Modify layout
Yes
TAPE OUT

Figure 7



MOS transistor (c) parameters:

L=L1
WF=W1
NF=3
DIFFL=A1
DIFFM=B1
DIFFR=C1

MOS transistor (d) parameters:

L=L2
WF=W2
NF=2
DIFFL=A2
DIFFM=B2
DIFFR=C2